REMARKS

The Official Action dated March 15, 2004 has been received and its contents carefully noted. In view thereof, claim 1 has been amended in order to better define that which Applicants regard as the invention. As previously, claims 1-3 are presently pending in the instant application.

With reference now to the Official Action and particularly page 2 thereof, claims 1-3 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Specifically, the Examiner notes that claim 1 recites the limitation "said bonding wire" on line 17 and there is insufficient antecedent basis for such limitation.

As can be seen from the foregoing amendments, independent claim 1 has been amended in order to better define that which Applicants regard as the invention. Moreover, independent claim 1 has been amended to delete the phrase referred to by the Examiner. Accordingly, with the foregoing amendments it is respectfully submitted that independent claim 1 as well as claims 2 and 3 which depend therefrom are now in proper formal condition for allowance.

Referring now to paragraph 8 of the Office Action, claims 1-3 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,930,599 issued to Fujimoto et al. This rejection is respectfully traversed in that the patent to Fujimoto et al. neither discloses nor suggests that which is presently set forth by Applicants' claimed invention.

More specifically, the present invention is directed to a method of manufacturing a semiconductor device comprising a first semiconductor chip provided with a first electrode on a first main surface and a second semiconductor chip provided with a second electrode on

a second main surface with the method including numerous steps wherein the second step comprises the step of arranging the distance from the first main surface of each first semiconductor chip in the semiconductor wafer to a surface of each second semiconductor chip opposite to the second main surface to be smaller than the distance from the first main surface of each first semiconductor chip in the semiconductor wafer to the highest position of the bonding wire on the first main surface. That is, the distance T_{chip} from the main surface of the first chip 101 to the back surface of the second chip 104 is smaller than the distance T_{WB} from the main surface of the first chip 101 to the highest position of the bonding wire 111 as particularly illustrated in Fig. 3, a copy of which is attached hereto.

Even if the back surface of the second chip 104 is polished to reduce the thickness of the semiconductor device, as long as the back surface of the second chip 104 is higher than the highest position of the bonding wire 111, the thickness of the semiconductor device will be determined by the height of the back surface of the second chip 104. However, if the back surface of the second chip 104 is lower than the highest position of the bonding wire 111, such as is the case with the present invention, the thickness of the semiconductor device will be determined by the highest position of the bonding wire 111. In other words, if the back surface of the second semiconductor chip 104 is being polished to a height lower than the highest position of the bonding wire 111 the thickness of the semiconductor device can be reduced to the limit of the wire bonding technology.

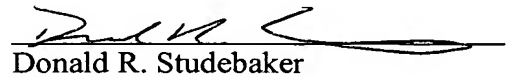
In rejecting Applicants' claimed invention, the Examiner asserts on page 4 of the Official Action that Fujimoto et al. teaches a distance between the first main surface of the first chip and the surface of the second chip opposite the first main surface to be smaller than the distance between the first main surface of the first chip and the highest position of the bonding wire as seen in Fig. 2C. However, this is not the case. With reference to Fig. 2C of

the Fujimoto et al. reference, a copy of which is attached hereto for the Examiner's convenience, it is clear that with respect to Applicants' claimed invention as set forth in independent claim 1 as amended, the distance T_1 from the main surface of the first chip 10 to the back surface of the second chip 20, the surface opposite the main surface of the second chip is clearly larger than the distance T_2 from the main surface of the first chip 10 to the highest position of the bonding wire 33. Accordingly, it is respectfully submitted that Applicants' claimed invention as set forth in independent claim 1, as amended, clearly distinguishes over the teachings of Fujimoto et al. That is, unlike Applicants' claimed invention, the thickness of the semiconductor device of Fujimoto et al. is dictated by the height of the back surface of the second chip 20 and not by the position of the bonding wire as is the case with Applicants' claimed invention. Accordingly, it is respectfully submitted that Applicants' claimed invention as set forth in independent claim 1, as amended, clearly distinguishes over the teachings of Fujimoto et al. Further, it is respectfully submitted that claims 2 and 3 which depend therefrom are likewise believed to be in proper condition for allowance.

Therefore, in view or the foregoing it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-3 be allowed and that the application be passed to issue.

Should the Examiner believe a further conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,



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